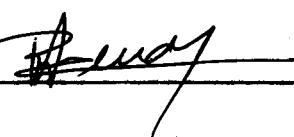



1. Publication Nº <i>INPE-4033-RTR/093</i>	2. Version	3. Date <i>Nov., 1986</i>	5. Distribution <input type="checkbox"/> Internal <input type="checkbox"/> External <input checked="" type="checkbox"/> Restricted
4. Origin <i>DCA/DIA</i>	Program <i>SUBORD</i>		
6. Key words - selected by the author(s) <i>TELEMETRY ENCODER - DATA ACQUISITION</i> <i>TELEMETRY FORMAT - PSK MODULATION</i>			
7. U.D.C.: <i>621.398</i>			
8. Title <i>THE DIRECT TELEMETRY ENCODER: A DETAILED DESCRIPTION</i>		10. Nº of pages: <i>39</i>	
		11. Last page: <i>A.15</i>	
		12. Revised by	
9. Authorship <i>Alderico R. de Paula Junior Ricardo de Azevedo Mendes Fernando Antonio Pessotta</i>	<i>Eduardo W. Bergamini</i> Eduardo W. Bergamini		
Responsible author 	13. Authorized by  Marco Antonio Raupp Director Geral		
14. Abstract/Notes <p><i>This document presents a detailed description of the Direct Telemetry Encoder for the data collection satellite. The Encoder acquires 72 digital and 96 analog telemetry signals from the satellite subsystems.</i></p> <p><i>The acquired data is formatted in a 128 octet frames.</i></p> <p><i>The telemetry frames are continuously generated producing a bit stream of 2048 bps. The bit string is biphase encoded and modulates a 65.536 kHz square wave subcarrier in PSK, producing the telemetry video that is sent to S-band transponder.</i></p>			
15. Remarks			



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TÍTULO

A DETAILED DESCRIPTION

CÓDIGO O.T.

[Empty box for O.T. code]

PREPARADO POR

APROVAÇÕES

ASS. Alderico R. de Paula Jr. DATA 21/07/86
 NOME Alderico R. de Paula Jr. DATA

ASS. Alderico R. de Paula Jr. DATA 21/07/86
 NOME Alderico R. de Paula Jr. DATA

ASS. Ricardo de A. Mendes DATA / /
 NOME Ricardo de A. Mendes DATA

ASS. Eduardo W. Bergamini DATA 04/08/86
 NOME Eduardo W. Bergamini DATA

ASS. Fernando Antonio Pessotta DATA 21/07/86
 NOME Fernando Antonio Pessotta DATA

ASS. _____ DATA / /
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DIRECT TELEMETRY ENCODER

1 - INTRODUCTION

Basically the Direct Telemetry Encoder (CODIR) is a unit that acquires telemetry signal, formats the acquired telemetry in frames and sends them to the S-Band transponder and the umbilical connector.

The data from the subsystems is sent to two sets of multiplexers both inside the CODIR. The first set is controlled by the CODIR and the second one is controlled by the UAC of the UPD/C which receives the corresponding multiplexed output.

The telemetry data acquired from the subsystems by the multiplexer under CODIR control is formatted in a 128 octet frame as depicted in Figure 1.

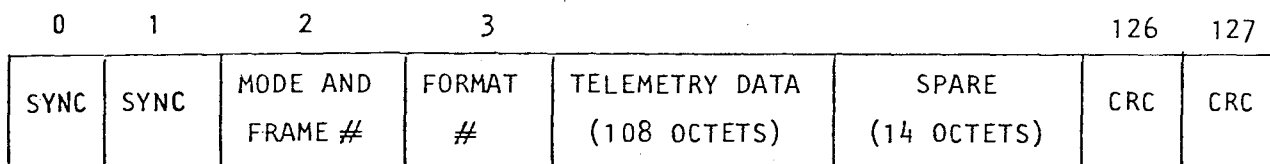


Fig. 1 - CODIR Telemetry Frame

The telemetry frames are continuously generated at a rate of two frames per second producing a bit stream of 2048 bps. The bit string is biphase encoded and modulates a 65.536 kHz square wave subcarrier in PSK, producing the telemetry video that is sent to the S-Band transponder and to the umbilical connector.

The CODIR consists of a controller, three Analog Interfaces and two Digital Interfaces. The block diagram of the CODIR is presented in Figure 2.

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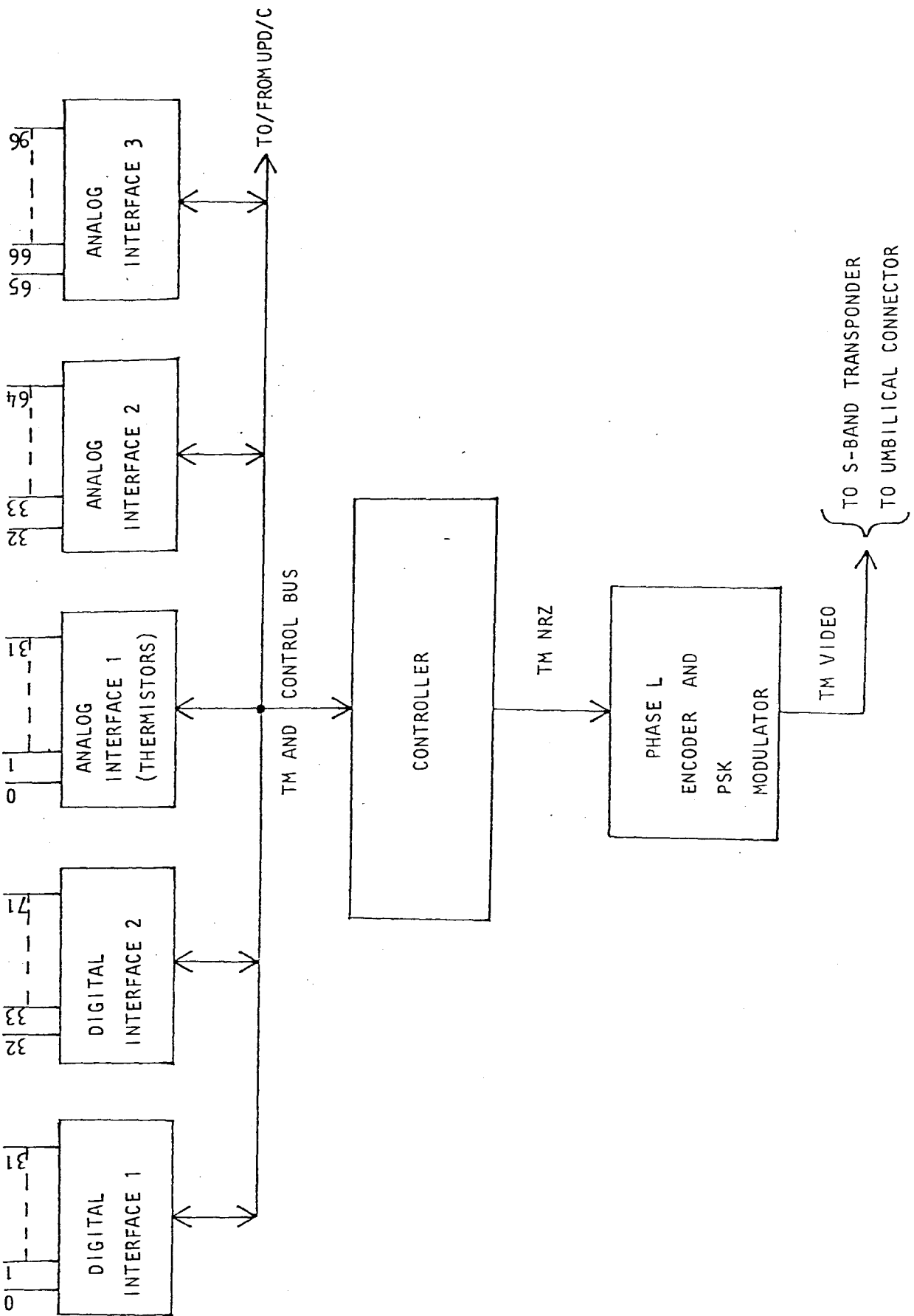


Fig. 2 - Direct Telemetry Encoder Block Diagram.



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2 - CONTROLLER

The controller provides the address for externa multiplexers, converts the analog telemetry signals in to digital ones and formats the acquired telemetry in frames, adding a header and CRC to the beginning and end of frame, respectively.

The block diagram of the controller is presented in Figure 3.

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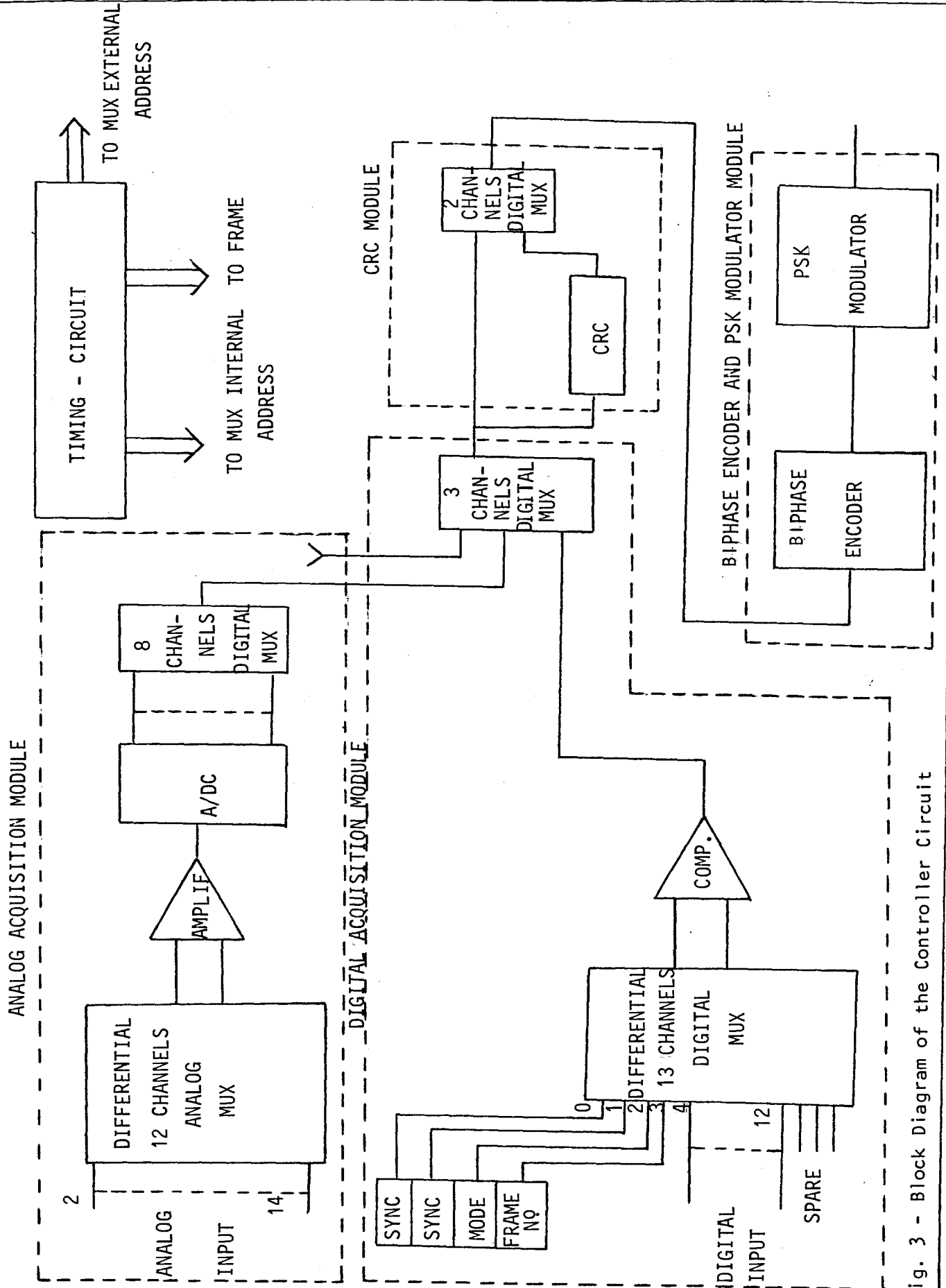


Fig. 3 - Block Diagram of the Controller Circuit

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2.1 - TIMING CIRCUIT

This circuit is composed of a 131.072 kHz oscillator and a set of counters that supply the internal and external multiplexer address and the 8 - bit frame number.

2.2 - ANALOG ACQUISITION MODULE

This module consists of 12 - channels differential analog multiplexers, an amplifier, an A/D converter and an 8 - bits digital multiplexer. Each analog input receives eight analog signals multiplexed in the analog interface. The differential multiplexer output is amplified to adapt the input signal level to the A/D converter.

The amplifier circuit is presented in Figure 4.

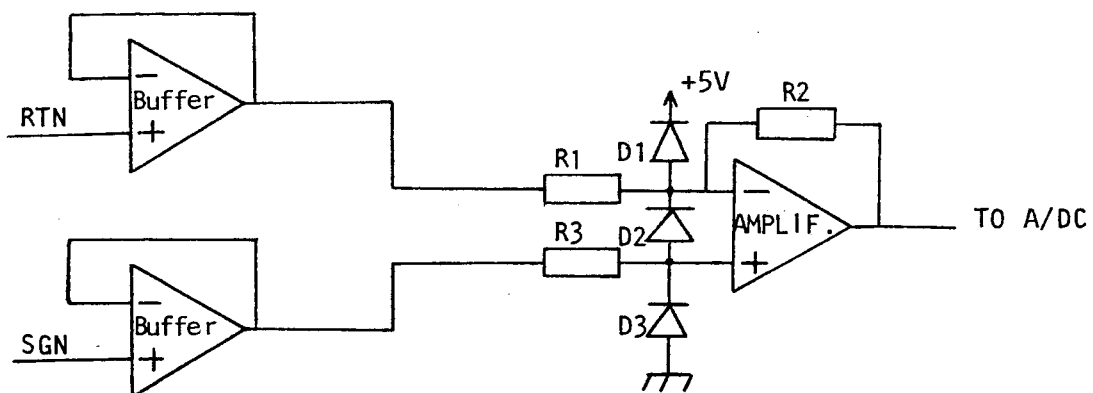


Fig. 4 - Diagram of Amplifier

The two voltage followers are utilized to provide a high input impedance. The input voltage is limited by the diodes and the gain of the differential amplifier is two.

The A/D converter is based on AD 571 manufactured by Analog Devices. This A/D is a 10 bits converter, but only the 8 most significative bits are used. The A/D input range is programed to 0v to 10v and the conversion time is 25 μ seg.

The A/D output is serialized by 8 channel digital multiplexers.

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2.3 - DIGITAL ACQUISITION MODULE

This module consists of a 9-channel differential analog multiplexer, a comparator circuit, four 8-channel digital multiplexers and a 3-channel digital multiplexer.

The four 8-channel multiplexers provide the synchronism word (16 bits), the mode (8 bits) and the frame number generated by the timing circuit.

Each input channel of the differential digital multiplexer receives 8 digital signals multiplexed in the digital interfaces.

The differential multiplexer outputs are applied to a comparator circuit, described in Figure 5.

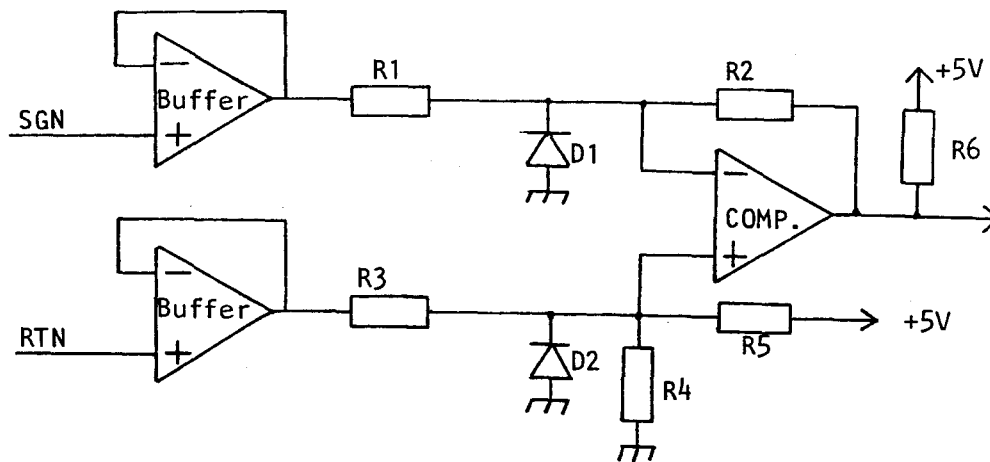


Fig. 5 - Diagram of Comparator Circuit.

The voltage followers are utilized to provide a high input impedance. The comparator is utilized to provide 2v of threshold to discriminate the digital levels.

The diodes protect the comparator against negative voltage.

The 3 channel digital multiplexers sequence the signal from digital and analog acquisition modules and spare signals (a 112 bits sequence of zeros and ones).

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2.4 - CRC MODULE

This circuit generates a 16-bit, cyclic redundant code word during the transmission of the telemetry frame to ground. The generation of the CRC begins as soon as the synchronism word is transmitted. The polynomial selected for the CRC is $G(x) = x^{16} + x^{12} + x^5 + 1$.

2.5 - BIPHASE ENCODER AND PSK MODULATOR MODULE

This circuit encodes the telemetry bit stream in a biphaser L using a clock of 2048 HZ (see Figure 6).

The glitches generated in this circuit are eliminated by flip-flop of the PSK modulator circuit.

The stream bit from biphaser encoder modulates a subcarrier of 65,536 KHz in PSK as presented in Figure 6.

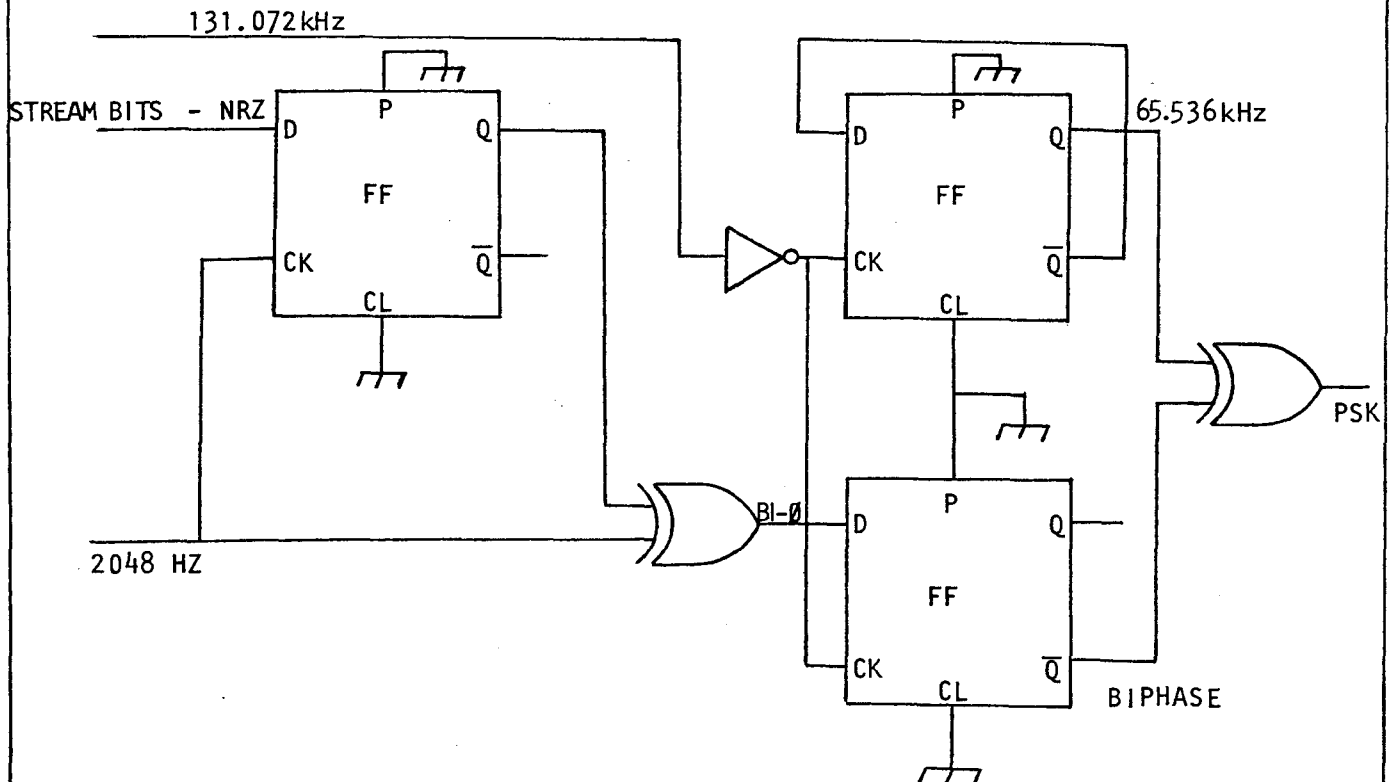


Fig. 6 - Diagram of BiPhase Encoder and PSK Modulator Circuits.



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The circuit and timing diagram of controller are presented in Appendix A.

3 - DIGITAL INTERFACE I

The Digital Interface I consists of two sets of 32-channels differential multiplexers. The first set is addressed by the CODIR controller, while the second set is addressed by UAC of the UPC. Each digital telemetry input is sent to the two set of multiplexers that can be energized and operated independently.

The 1 M Ω resistor in the input of the multiplexers are utilized to protect the input against over voltage and to isolate the multiplexers controlled by the CODIR from the multiplexers controlled by the UAC of the UPD/C.

The differential multiplexers are used in order to isolate the ground among the subsystems and to reject the common mode noise.

The Digital Interface I circuit is presented in Appendix A.

4 - DIGITAL INTERFACE II

The Digital Interface II is similar to Digital Interface I. The only difference is the number of input channels, that is 40.

This interface also contains the comparator circuits to receive the multiplex address from the UAC of the UPD.

The digital interface II circuit is presented in Appendix A.

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5 - ANALOG INTERFACE I

This interface is utilized to multiplex the 32 signals from the thermistors. In this interface, it is not necessary to multiplex the return of the thermistor because they have the same reference point. The thermistor circuits (Figure 7) are energized independently of the CODIR.

The Analog Interface I circuit is presented in Appendix A.

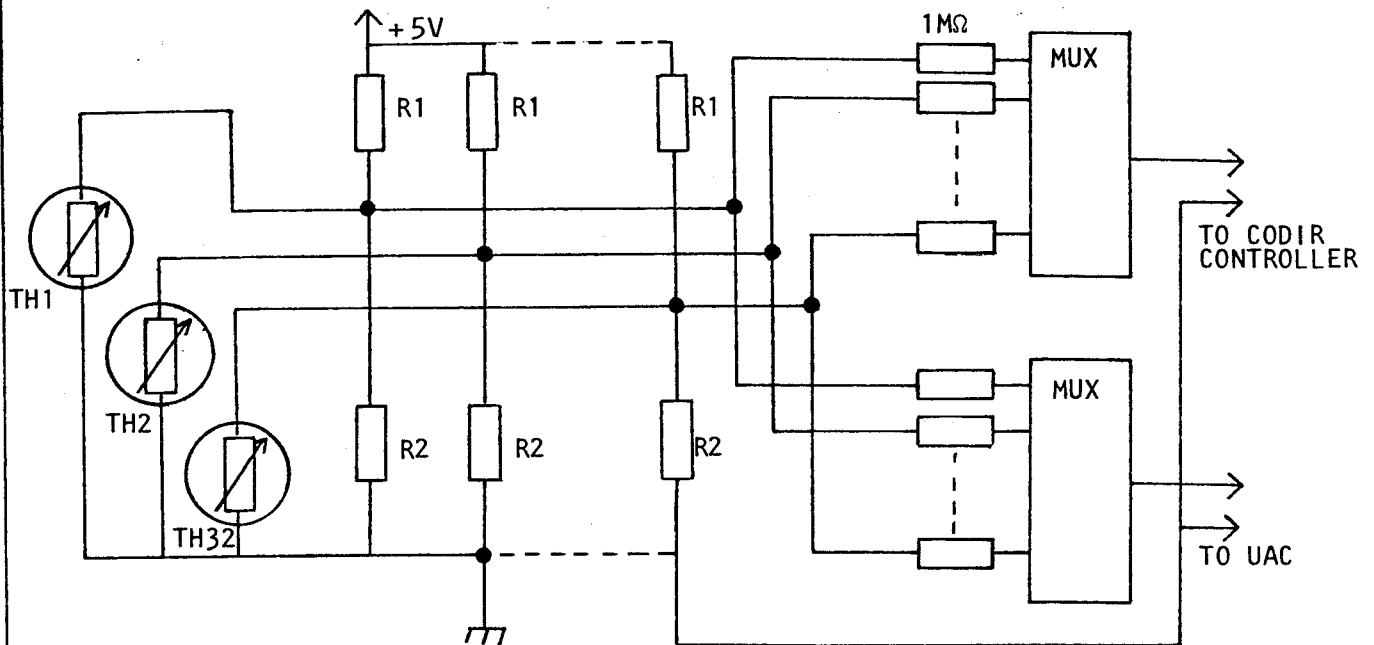


Fig. 7 - Temperature Acquisition Circuit.

6 - ANALOG INTERFACE II AND III

These interfaces are utilized to acquire the analog telemetry from subsystems. Each interface has the capability to acquire up to 32 channels.

In a similar way to the digital interface, the differential multiplexers are utilized to isolate the ground among the subsystems and to reject the common mode voice.

The Analog Interface II and III circuits are presented in Appendix A.



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COMPONENTS LIST OF CONTROLLER

QTY	DISCRIPTION OF COMPONENT	PART NUMBER
	Analog Digital Converter	AD571SD-883
	Cristal Oscillator CMOS Frecuence 131.072 kHz	CO.422D-2B
	3 Terminal Negative Regulators	LM79M05H03A
5	Diode High - Speed Switching	1N4148
	Resistor 5K1Ω; 1/8 W, 5%	
20	Resistor 10KΩ, 1/8 W, 5%	
5	Resistor 6K2, 1/8 W, 5%	
	Resistor 510KΩ, 1/8 W, 5%	
2	Resistor 2,5MΩ, 1/8 W, 5%	
	Resistor 5,1 MΩ, 1/8, 5%	
	Disc Ceramic Capacitor 33PF	
10	Disc Ceramic Capacitor 100 KPF	
3	D- Type Flip-Flop	4013B
6	Binary with asynchronous clear	40161B
5	8 Channel Data Selector	4512B
8	Analog Multiplexer/Demultiplexer	4051B
2	Quad Exclusive - or Gate	4070B
3	Nand Gates Quad 2 - INPUT	4011B
	And Gate Triple 3-input and Gate	4073B
2	Dual 4 - Stage Static Shift Register	4015B
	8 - Input nor/or Gate	4078B
	8 - Input Nand/and Gate	4068B
	Hex High-to-Low voltage (inverter)	4049VB
	Low Power Low off set voltage Quad Comparator	LM139AJ14A
4	Voltage Follower CER. Dip	LM110J14A
	Operational Amplifier	LM101AJ14A



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COMPONENTS LIST OF DIGITAL I INTERFACE

QTY	DESCRIPTION OF COMPONENT	NUMBER PART
18	Analog Multiplexer/Demultiplexer	4051B
	3 - Terminal Negative Regulators	LM79M05H03A
128	Resistor $1M\Omega$, 1/8W, 5%	
	FC Printed Circuit Board Connectors	FC0801-120-00
6	Resistor $2K\Omega$, 1/8W, 5%	
6	Resistor $3K\Omega$, 1/8W, 5%	
6	Disc Ceramic Capacitor 220 PF	
6	Disc Ceramic Capacitor .33MF	
6	Disc Ceramic Capacitor .1MF	



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COMPONENTS LIST OF DIGITAL II INTERFACE

QTY	DESCRIPTION OF COMPONENT	NUMBER PART
22	Analog Multiplexer/Demultiplexer	4051B
2	Low Power Low off set voltage Quad Comparators	LM139AJ14A
	Nand Gates Quad 2 Inputs	4011B
14	Resistor 5K1Ω, 1/8W, 5%	
21	Resistor 10KΩ, 1/8W, 5%	
160	Resistor 1MΩ, 1/8W, 5%	
	Disc Ceramic capacitor .33MF	
	Disc Ceramic capacitor .1MF	
	FC Printed Circuit Board Connectors	FC0801-120-00



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COMPONENTS LIST OF ANALOG I INTERFACE

QTY	DESCRIPTION OF COMPENENT	NUMBER PART
10	Analog Multiplexer/Demultiplexer	4051B
32	Thermistor	
66	Resistor 1M Ω , 1/8 W, 5%	
32	Resistor , 1/8 W, 5%	
32	Resistor , 1/8 W, 5%	
	F.C. Printed Circ. Board Connectors	FC0801-120.00



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COMPONENTS LIST OF ANALOG II INTERFACE

QTY	DESCRIPTION OF COMPONENT	NUMBER PART
18	Analog Multiplexer/Demultiplexer Single 8 - Channel	4051B
128	Resistor 1M Ω , 1/8 W, 5%	



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COMPONENTS LIST OF ANALOG III INTERFACE

QTY	DESCRIPTION OF COMPONENT	PART NUMBER
18	Analog Multiplexer/Demultiplexer Single - 8 channel	
128	Resistor 1M Ω , 1/8W, 5% FC Printed Circ. Board Connectors	FL0801-120-00



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WIRING, CABLING SUBSYSTEM AND CONNECTORS AND ACCESSORIES

QTY	DESCRIPTION OF COMPONENT	PART NUMBER
6	Stranded Hook-up wires 26 AWG For Signal Lines Stranded Hook-up wires 22 AWG For Power Lines Rectangular D Subminiature Rectangular D Subminiature Nylon Potting Shells Nylon Potting Shells Switching Shells Switching Shells Screw Lock assembly	MD308N50P1 MD308N37P1 DD50908-1 DC50907-1 DD19678-9 DC19678-8
6	FD Printed Circuit Board Connector (Receptor)	FD0301-120.00

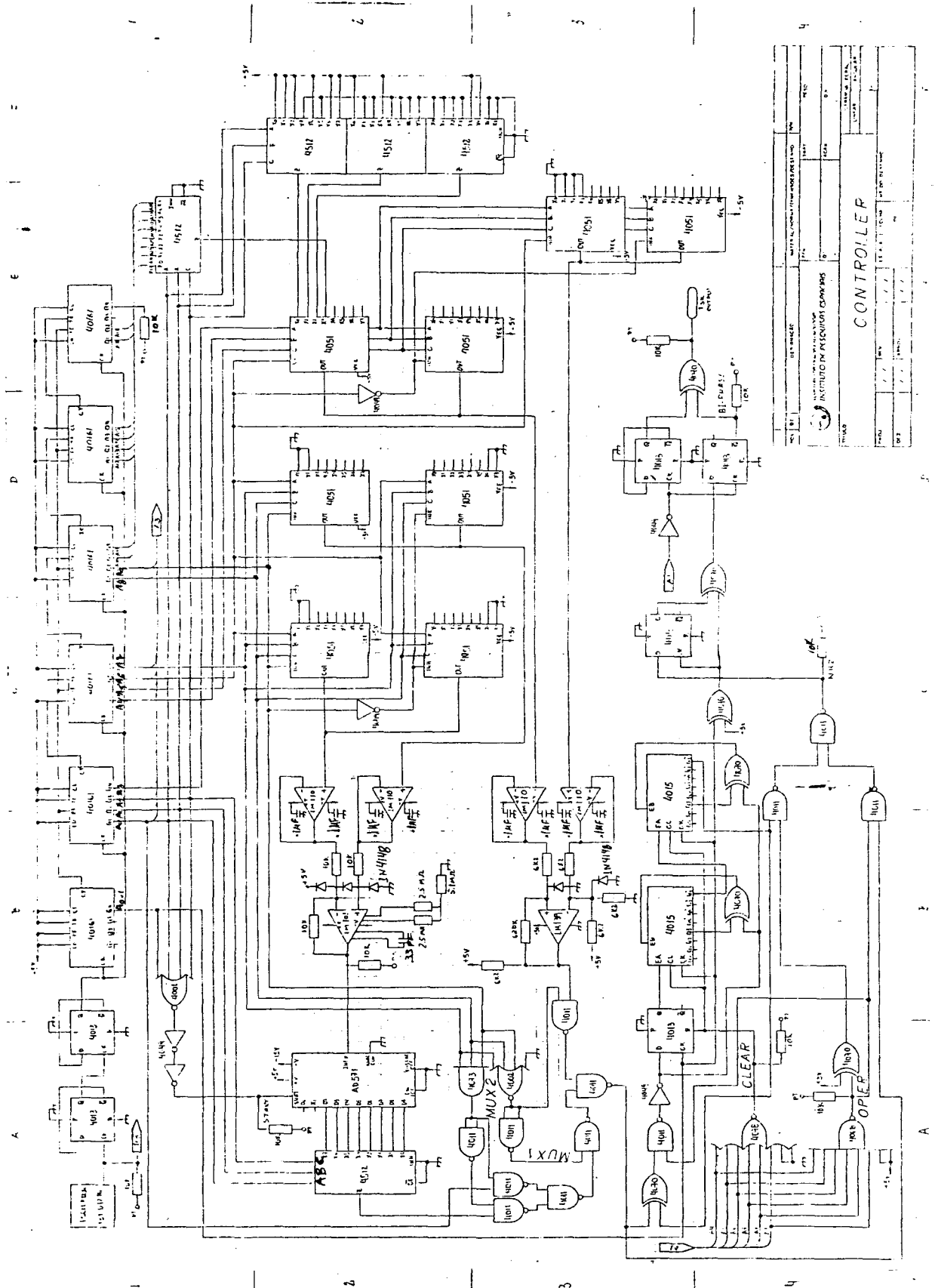


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APPENDIX A

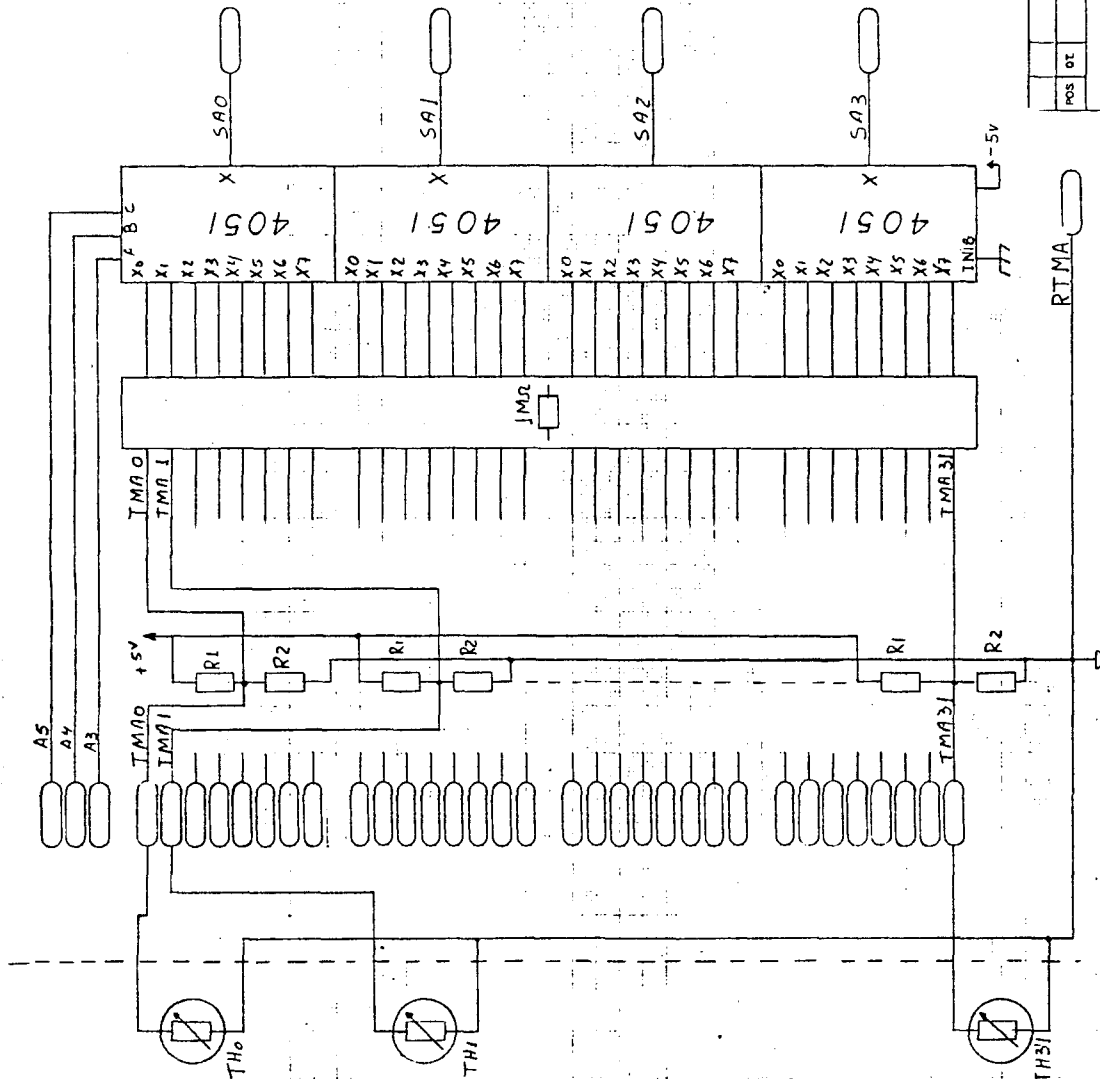
ELECTRIC DIAGRAMS

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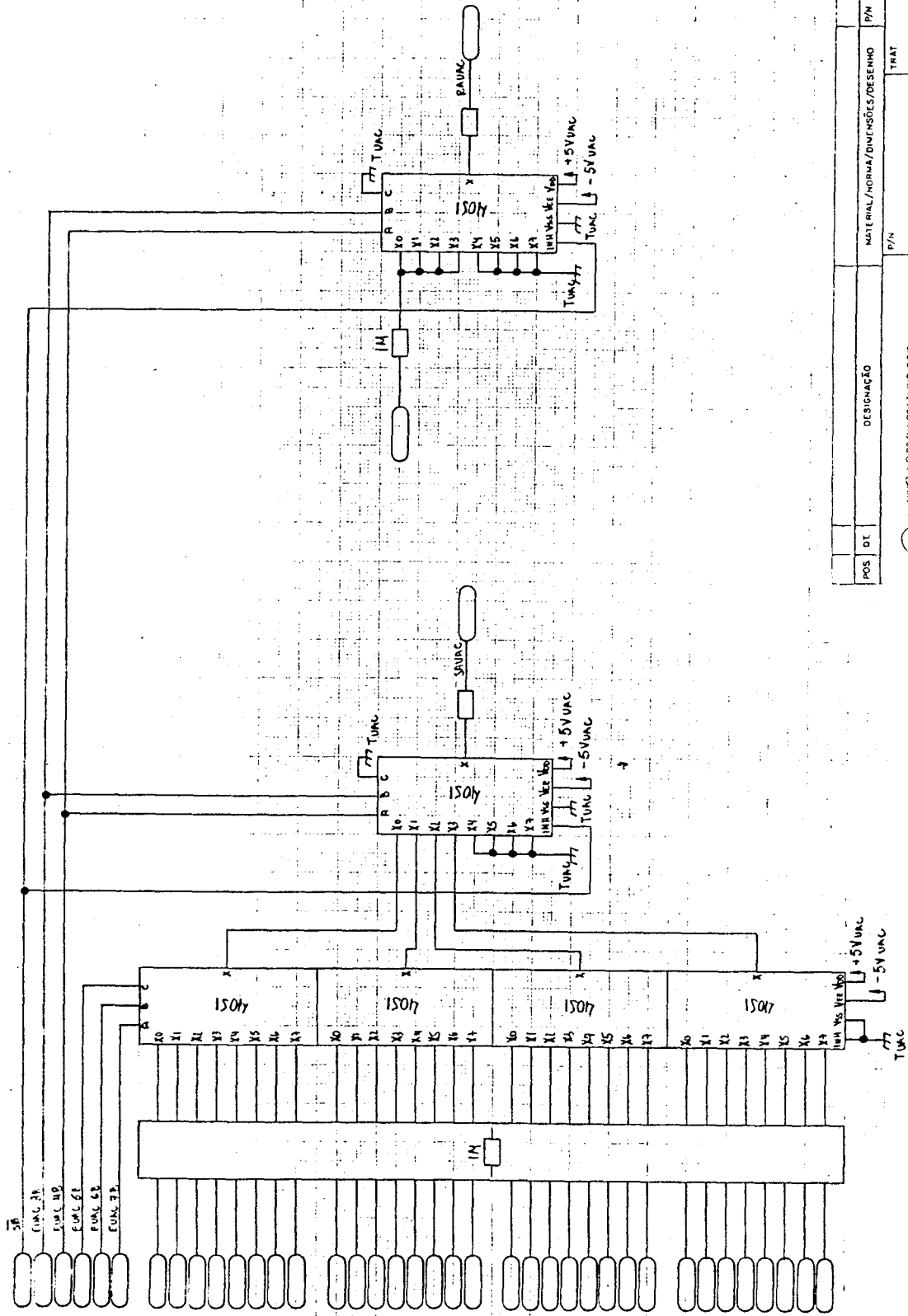


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						03
				OT	ACAB	

TOLERÂNCIA GERAL		TOLERÂNCIA ANGULAR	
LINEAR	ANGULAR	LINEAR	ANGULAR

TÍTULO			
ANALOG INTERFACE I			
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/ /	/ /	/ /	/ /
DES	APROV		
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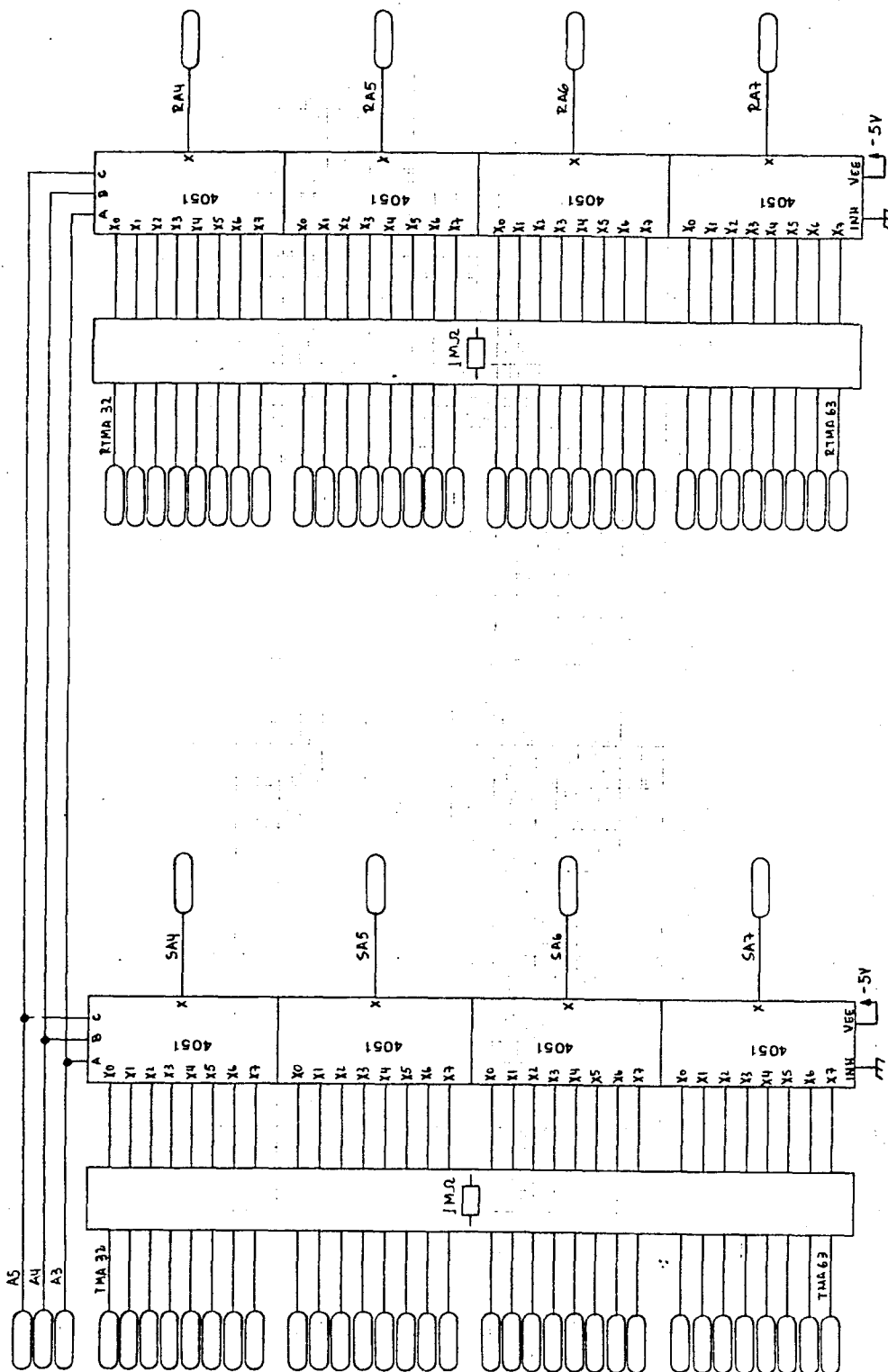
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		DI.	NCAB
			CS
			TOLERÂNCIA
			LINEAR
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TÍTULO	INTERFACE I		
TPHOU	REV	ESCALA	FOLHA
DES	APROV	DE	Nº DO DESENHO



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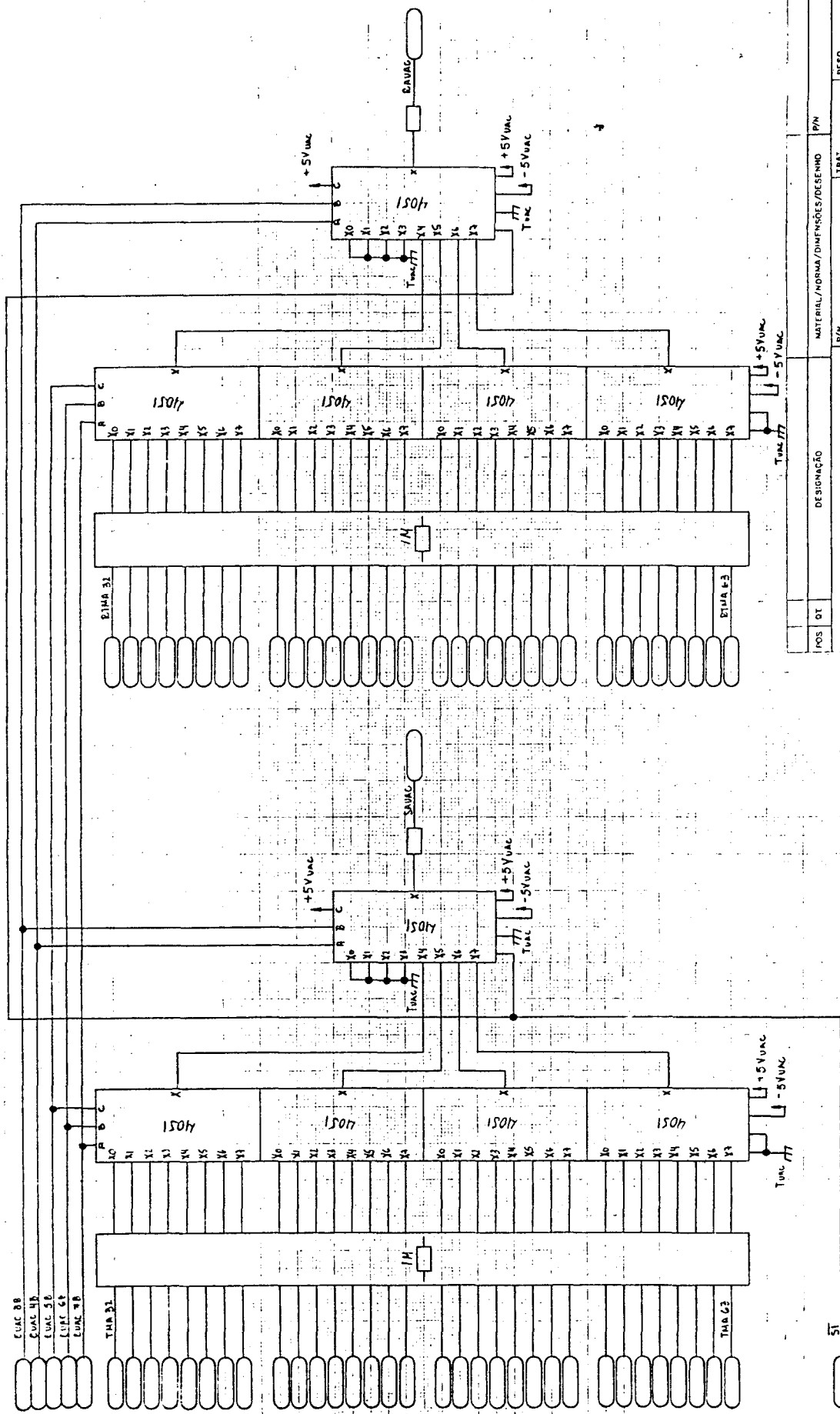


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		ACAB.	0 5
		OT.	
INSTITUTO DE PESQUISAS ESPACIAIS MINISTÉRIO DA CIÊNCIA E TECNOLOGIA		TOLERÂNCIA GERAL LINEAR ANGULAR	
TÍTULO			
ANALOG INTERFACE II			
PROJ	REV	ESCALA	FOLHA Nº DO DESENHO
DES	APROX	///	OE

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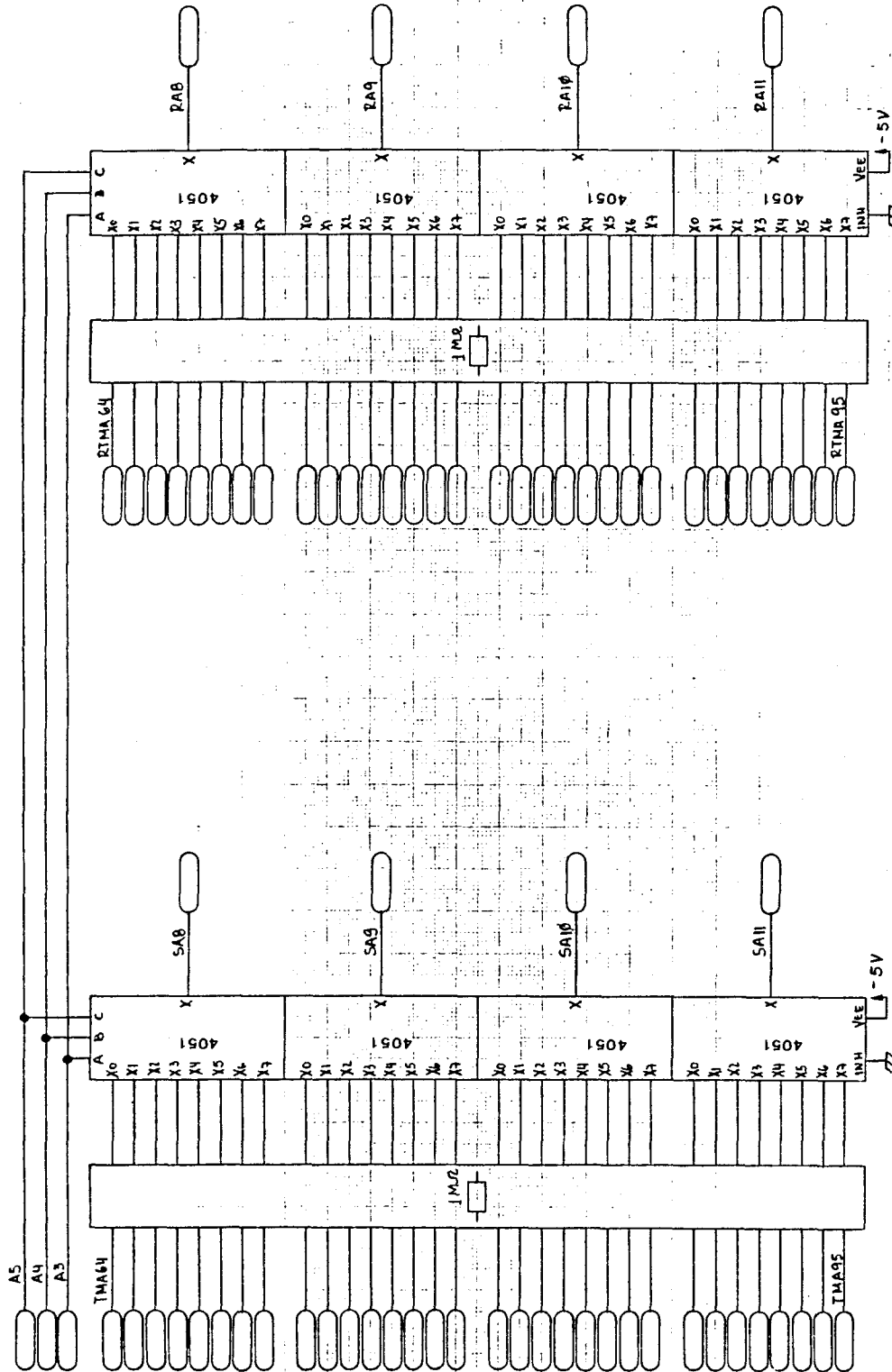
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		DE		PESO	
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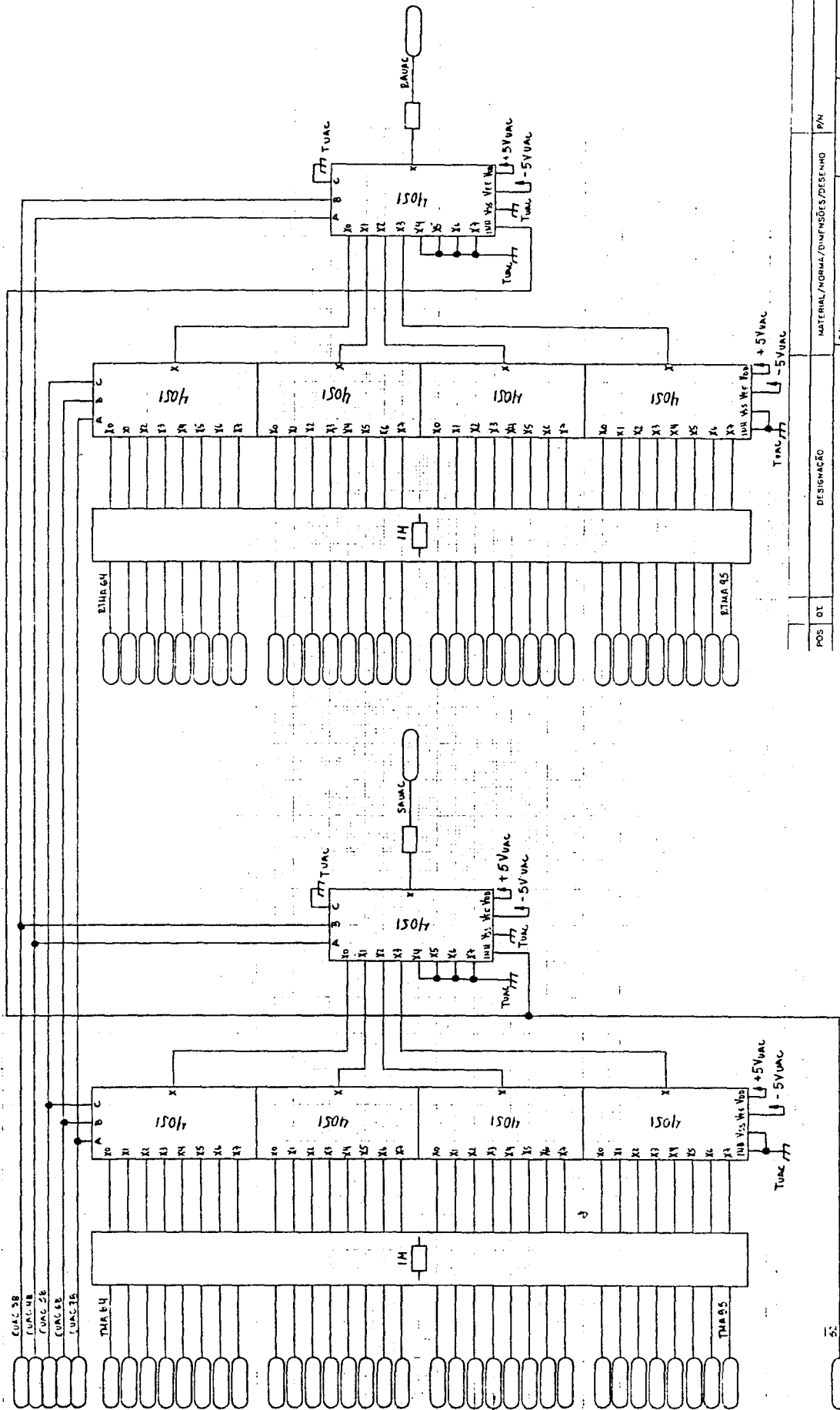


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ANALOG INTERFACE III						
TÍTULO: ANALOG INTERFACE III						
PROJ	DES	REV	ESCALA	FOLHA	Nº DO DESENHO	
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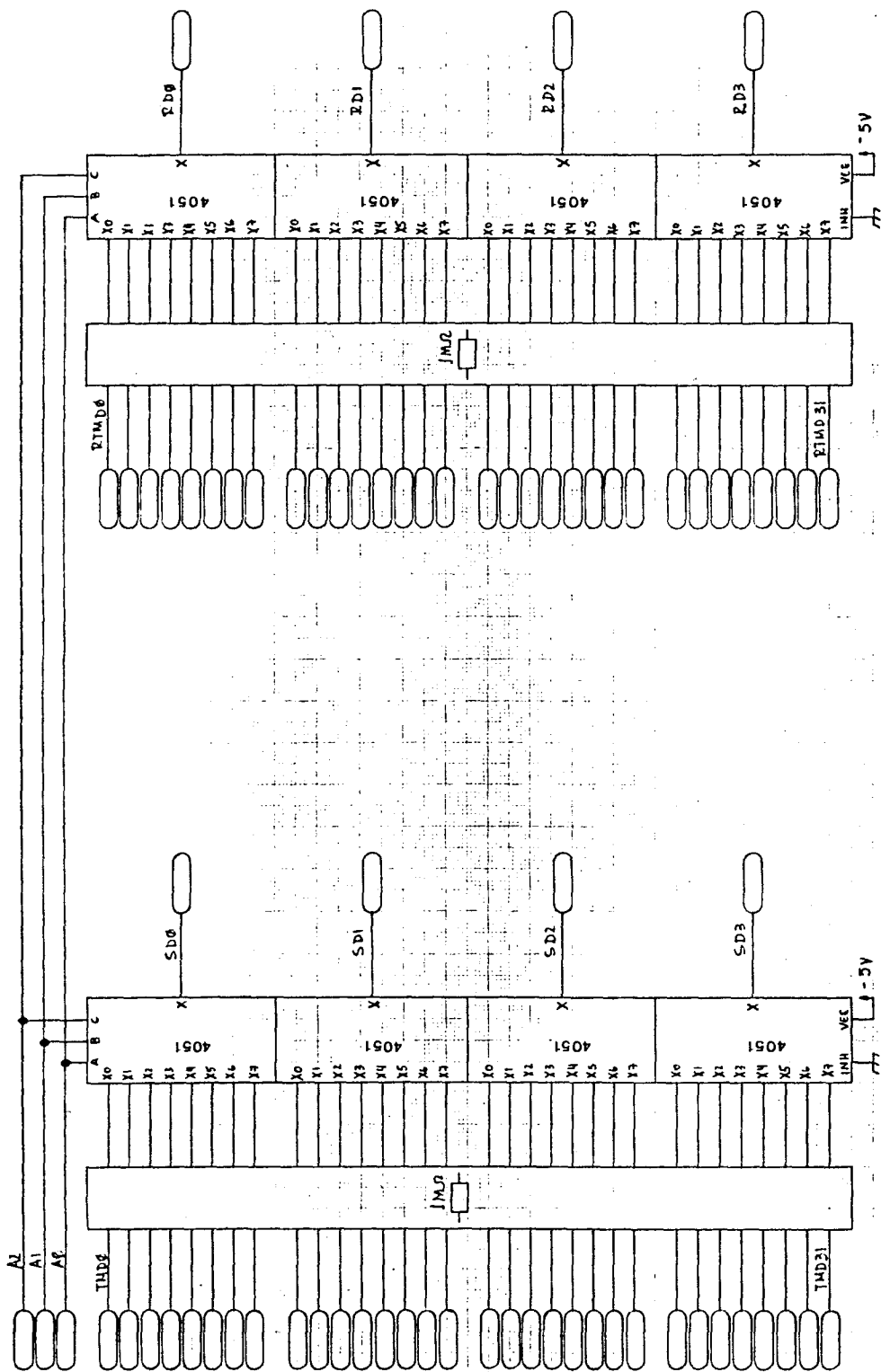


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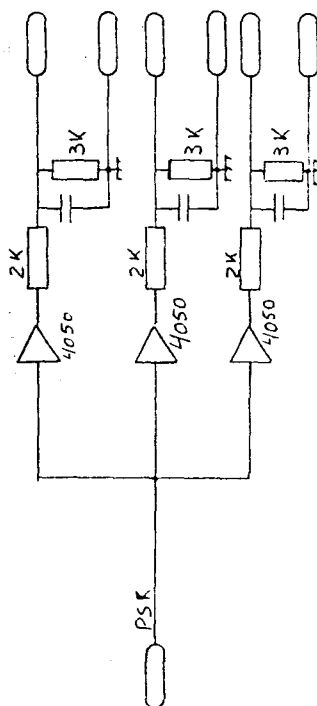
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DES	APROV		DE



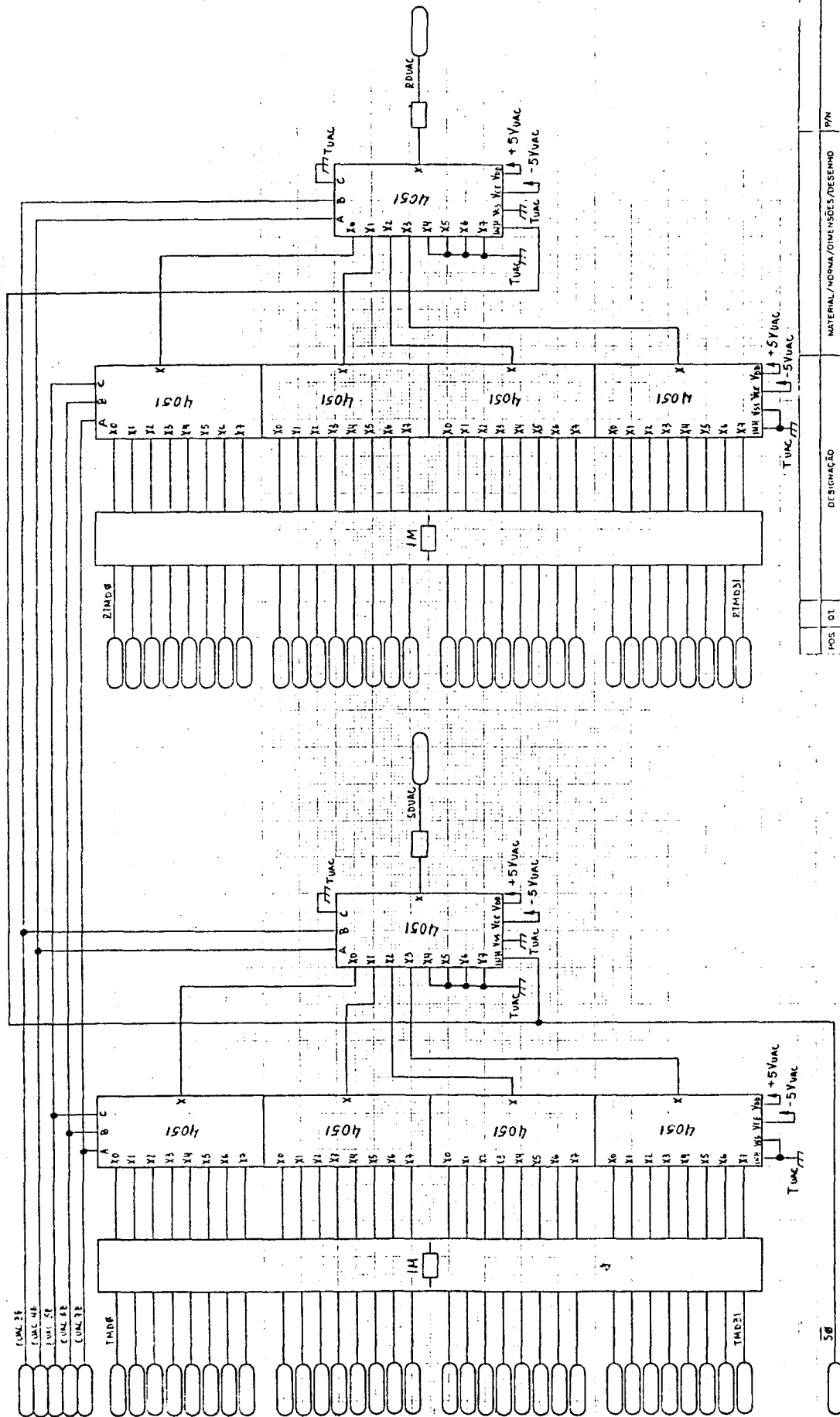
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				DE		

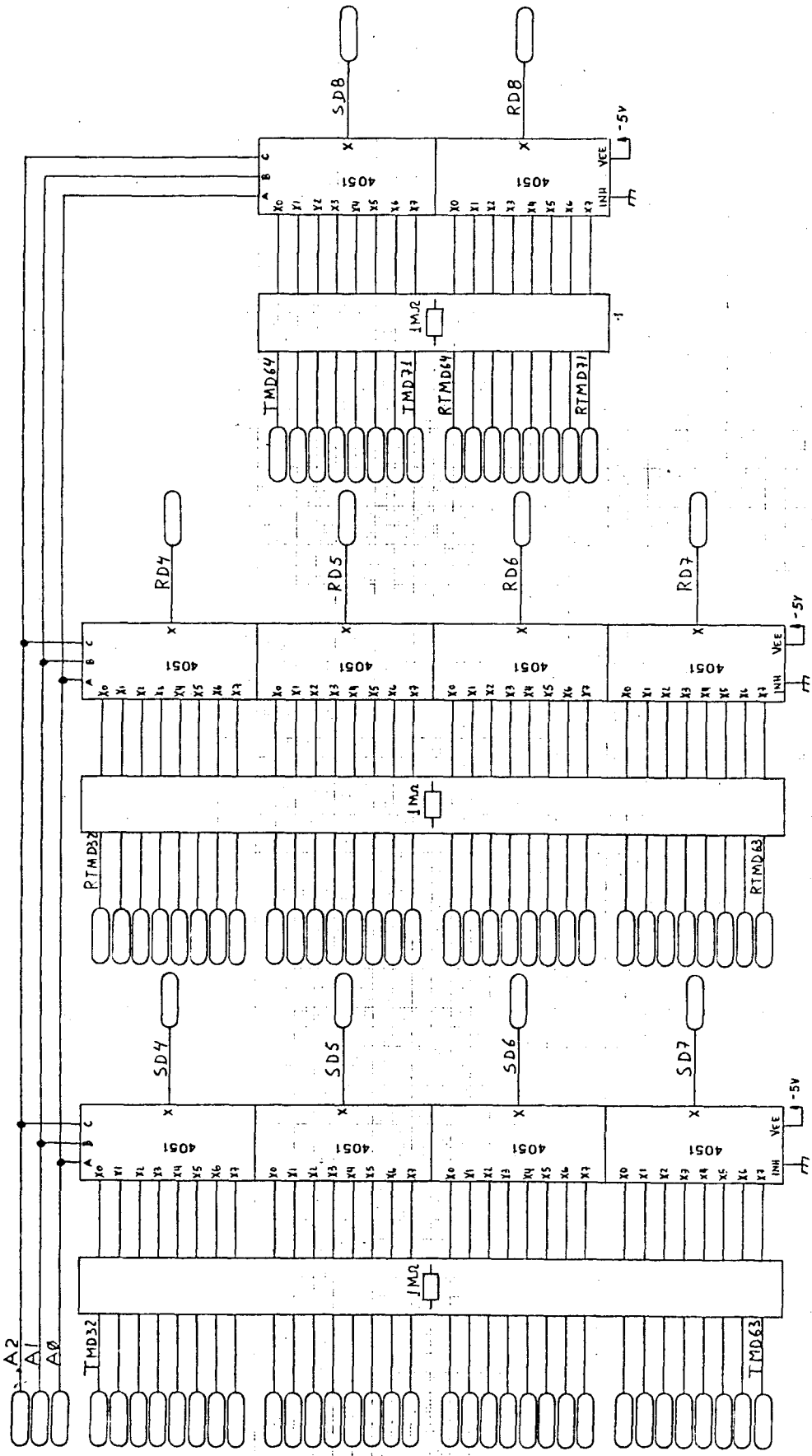


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DIGITAL INTERFACE I						
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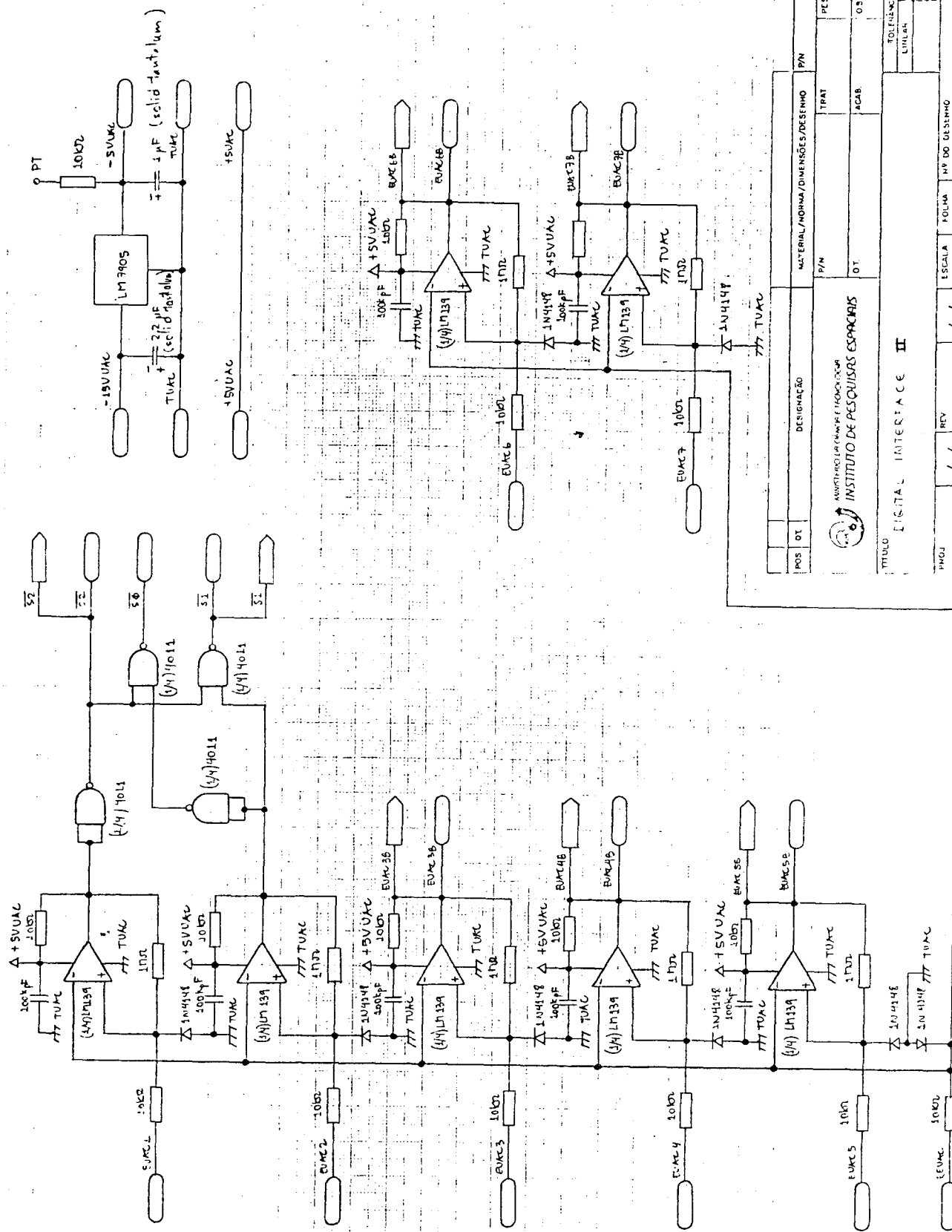
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INSTITUTO DE PESQUISAS ESPACIAIS TÍTULO: DIGITAL INTERFACE II					
PROJ.	REV.	ESCALA	FOLHA	Nº DO DESINHO	TOLERÂNCIA GERAL
DES	APROV.		DE		LINEAR / ANGULAR



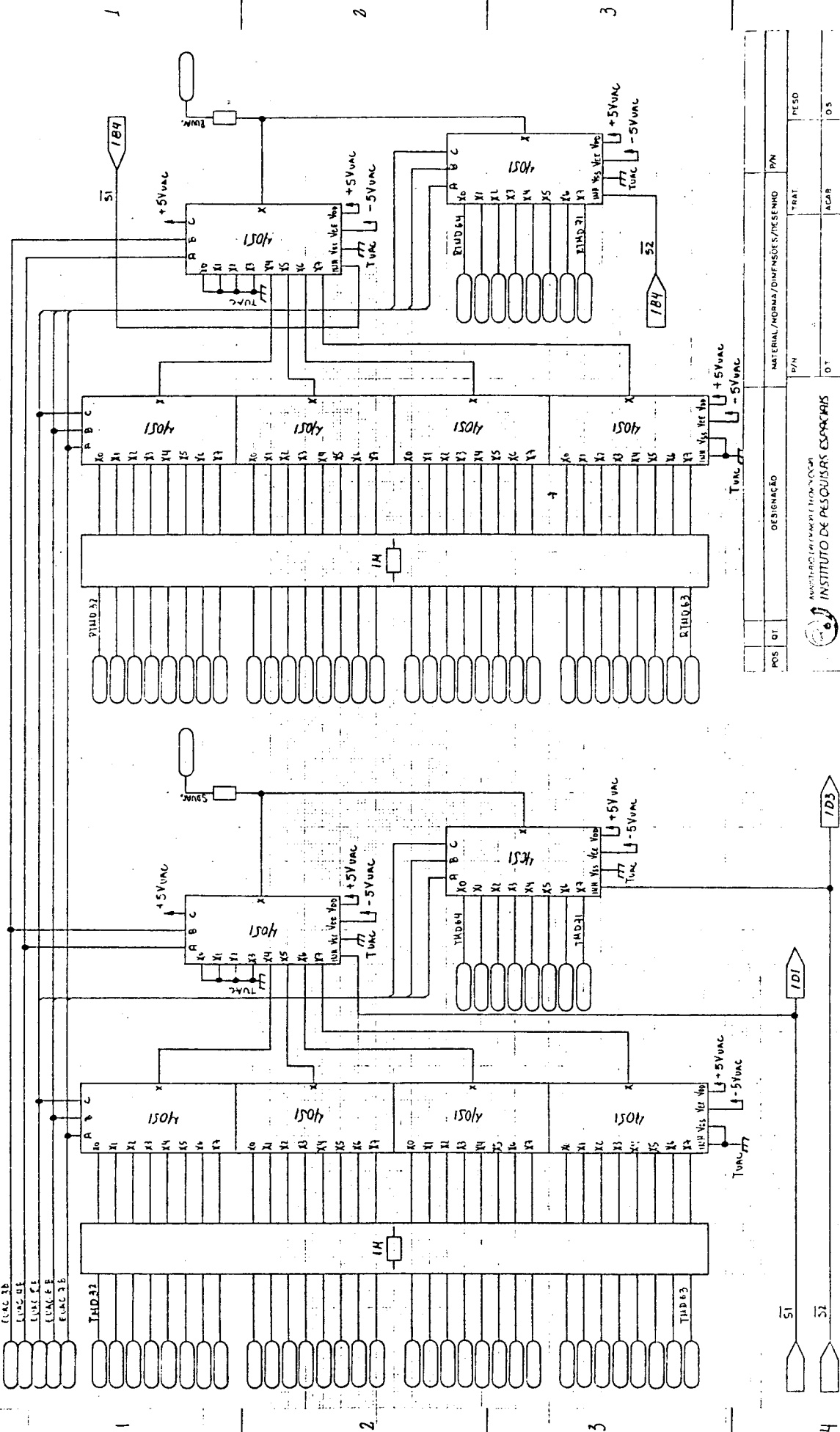
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DESIGNAÇÃO	MATERIAL/NORMA/DIMENSÕES/DESENHO		
POS	DT	P/N	P/N
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TÍTULO			
DIGITAL INTERFACE II			
PROJ	REV	ESCALA	FOLHA Nº DO DESINHO
DA S	///	///	DE
	///	///	
TOLERÂNCIA GERAL		PESO	OS
LINEAR		ACAB	
FURTO			



MECB/SS



POS	DT	DESIGNAÇÃO	MATERIAL/NORMA/DIMENSÕES/PESQUENHO	P/N	TRAT	PESO
					ALGAR	0,5

TITULO		ESCALA		FOLHA		Nº DO DESENHO	
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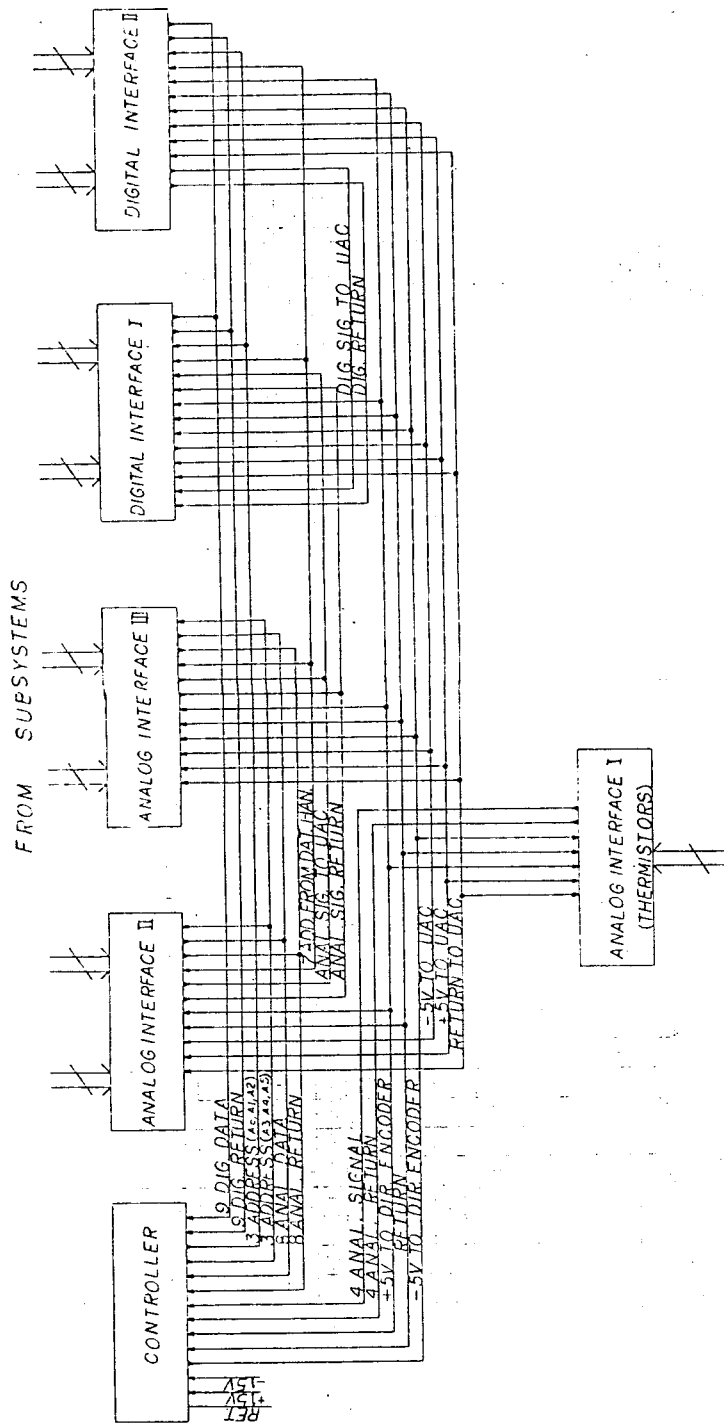
TOLERANÇAS GERAIS	
LINEAR	ANGULAR

INSTITUTO DE PESQUISAS ESPACIAIS

DIGITAL INTERFACE II



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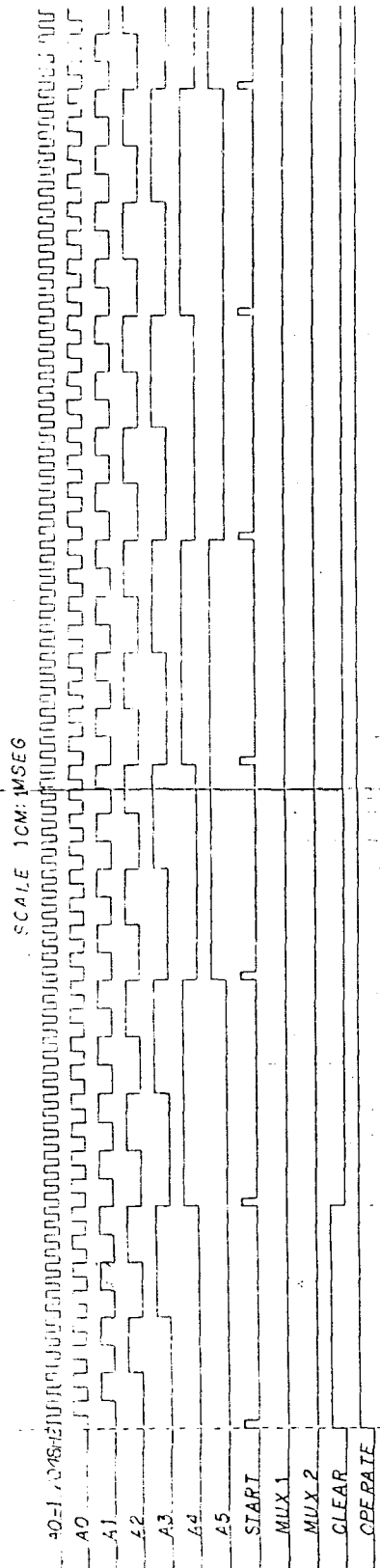


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INTERCONNECTION BETWEEN INTERFACES		INTERCONNECTION BETWEEN INTERFACES	
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INSTITUTO DE PESQUISAS ESPACIAIS		INSTITUTO DE PESQUISAS ESPACIAIS	

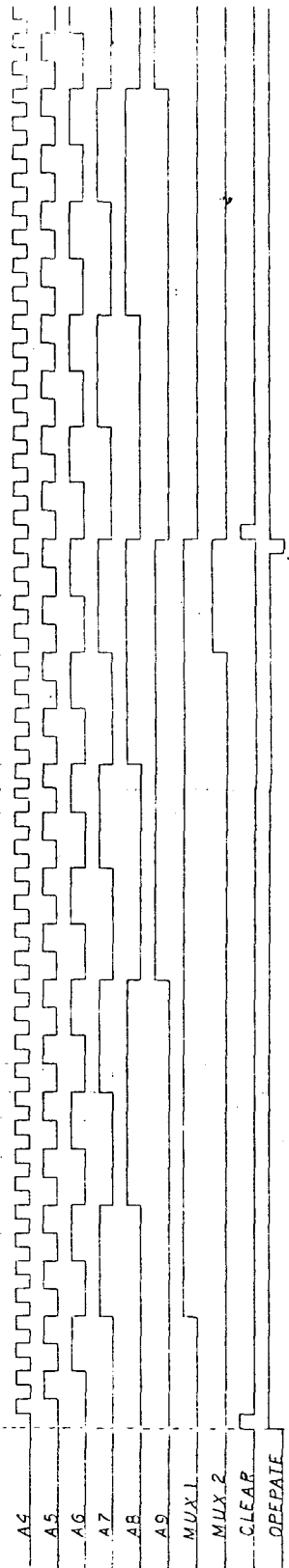


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TIMING DIAGRAM



SCALE 1CM: 6MSEG



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INSTITUTO DE PESQUISAS ESPACIAIS			
CONTROLER TIMING DIAGRAM			
INSTITUTO DE PESQUISAS ESPACIAIS			



PROPOSTA PARA PUBLICAÇÃO

DATA
 31.07.86

IDENTIFICAÇÃO	TÍTULO	
	THE DIRECT TELEMETRY ENCODER : A DETAILED DESCRIPTION	
	AUTORIA	PROJETO/PROGRAMA
	Alderico R. de Paula Junior Ricardo de Azevedo Mendes Fernando Antonio Pessotta	SUBORD
	DIVISÃO	
	DIA	
	DEPARTAMENTO	
	DCA	
DIVULGAÇÃO <input type="checkbox"/> EXTERNA <input checked="" type="checkbox"/> INTERNA MEIO: Restrita		

REVISÃO TÉCNICA	REVISOR TÉCNICO	APROVADO: <input checked="" type="checkbox"/> SIM <input type="checkbox"/> NÃO <input type="checkbox"/> VER VERSO	APROVAÇÕES
	<i>Eduardo W. Bergamini</i>	<u>4/11/86</u> DATA <i>Alderico R. de Paula Junior</i> CHEFE DIVISÃO	
	RECEBI EM: _____ REVISADO EM: _____		
	OBSERVAÇÕES: <input type="checkbox"/> NÃO HÁ <input type="checkbox"/> VER VERSO	APROVADO: <input type="checkbox"/> SIM <input type="checkbox"/> NÃO <input type="checkbox"/> VER VERSO	
	DEVOLVI EM: _____	<u>4/11/86</u> DATA <i>Eduardo W. Bergamini</i> CHEFE DEPARTAMENTO	
	<i>Eduardo W. Bergamini</i> Chefe do Dept. de Aplicações Espaciais	<i>Eduardo W. Bergamini</i> Chefe do Dept. de Aplicações Espaciais	

REVISÃO DE LINGUAGEM	Nº : <u>332</u>	PRIORIDADE: <u>1</u>	DATILOGRAFIA	
		DATA: <u>1-8-86</u>		O(S) AUTOR(ES) DEVE(M) MENCIONAR NO VERSO, OU ANEXAR NORMAS E/OU INSTRUÇÕES ESPECIAIS
	REVISADO	<input type="checkbox"/> COM <input type="checkbox"/> SEM		RECEBIDO EM: <u>Julho/86</u>
		<input type="checkbox"/> CORREÇÕES <input type="checkbox"/> VER VERSO	CONCLUÍDO EM: <u>Julho/86</u>	
	POR: <i>Marta Prado de Carvalho</i>	<i>Marta Prado de Carvalho</i>	DATILOGRAFA: <u>Marta</u>	
	<u>4.8.86</u> DATA	<u>Marta Prado de Carvalho</u> ASSINATURA	<i>Marta Prado de Carvalho</i> ASSINATURA	

PARECER

FAVORÁVEL : SIM VER _____ DATA _____ RESPONSÁVEL/PROGRAMA

NÃO VERSO

EM CONDIÇÕES DE PUBLICAÇÃO EM: _____

AUTOR RESPONSÁVEL _____

AUTORIZO A PUBLICAÇÃO : SIM NÃO

DIVULGAÇÃO INTERNA EXTERNA MEIO: _____

OBSERVAÇÕES : _____

_____ DATA _____ DIRETOR

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